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TiO_2/HfO_2 Bi-Layer Gate Stacks Grown by Atomic Layer Deposition for Germanium-Based Metal-Oxide-Semiconductor Devices Using GeO_xN_y Passivation Layer

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Material and electrical properties of TiO_2/HfO_2 bi-layer gate stacks were investigated for germanium (Ge) based metal-oxide-semiconductor devices. In situ NH_3 plasma treatment was employed to passivate the Ge surface and promising performance including low capacitance-voltage hysteresis and interface trap density was achieved. It shows a superior dielectric breakdown voltage (4.2–3.4 V) for the TiO_2/HfO_2 bi-layer stacks than HfO_2 single layer stack at a similar capacitance equivalent thickness (CET) of 1.6 nm. A minimum CET of 1.4 nm was obtained for capacitors on both p and n-type Ge (100) with a gate leakage current density $< 4 \times 10^{-7}$ A/cm^2 at $V_{FB} \pm 1$ V.
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As Silicon based complementary metal-oxide-semiconductor field-effect-transistor (CMOSFET) is approaching its fundamental limit, alternative channel material germanium (Ge) has received intensive interests due to its intrinsic high mobility for both electrons (3900 cm^2/V s) and holes (1900 cm^2/V s).[1] Various high k gate dielectrics including Al_2O_3,[2,3] HfO_2,[4,5] and ZrO_2[6,7]have been investigated for Ge-based MOS devices. TiO_2 exhibits a high dielectric constant (~80 for the rutile crystalline phase)[8] and can be considered a potential candidate for a high-k dielectric.[9] However, its low conduction band offset (CBO) makes an additional interfacial layer (IL) with sufficient CBO necessary.[8] Both Al_2O_3 (Refs. 9 and 10) and HfO_2 (Ref. 11) IL have been investigated for implementing TiO_2 as gate dielectric on Ge. HfO_2 shows superior properties due to its higher k value and less degradation for ultrathin films.[11] Although the band gap of HfO_2 is smaller than Al_2O_3, both CBO and valence band offset (VBO) are already larger than 2 eV for HfO_2 with respect to Ge.[12] Among many thin film deposition techniques, atomic layer deposition (ALD) plays a major role for high k dielectrics deposition owing to its intrinsic advantage of growing uniform films with precise thickness control at atomic level. Comparing to conventional thermal ALD, plasma enhanced (PE)-ALD is considered a promising approach to deposit films at lower temperature with high quality and higher density due to the higher reactivity of radicals.[13] For instance, TiO_2 deposited by thermal ALD exhibits a k value in the range of 32–35 (Ref. 9) while the TiO_2 films grown by PE-ALD possess much higher k value (~50).[11] With our control samples, HfO_2 grown by PE-ALD also exhibits a higher k value than thermal ALD (24 vs. 18). Prior to high k dielectric deposition, Ge surface passivation is essential to reduce the interface trap density (D_{it}). Effective electrical Ge surface passivation has been demonstrated using a variety of methods, e.g., using GeO_2,[14,15] surface nitridation with thermal NH_3,[16] SiH_4-NH_3 (Ref. 17) or a $H_2/N_2/Ar$ (Ref. 18) gas plasma. While the thermal NH_3 treatment approach has been shown to be quite effective, it usually requires high temperature (e.g., >550°C) to form a high quality GeO_xN_y IL.[16] Recently, we reported the ultrathin GeO_xN_y passivation layer formed by NH_3 plasma, which can be performed at ALD process temperature (e.g., 250°C).[19] It is promising to limit the total thermal budget by using this plasma passivation technique. In this work, we investigate the properties of TiO_2 and HfO_2 films grown by PE-ALD on Ge (100) after in situ GeO_xN_y passivation with NH_3 plasma. Electrical performance of the capacitors with TiO_2/HfO_2 bi-layer gate stacks is comprehensively evaluated.

Ge (100) wafers with resistivity of 0.05–0.1 Ω cm were used as substrates. Prior to 5 min rinse in de-ionized water, the Ge wafers were cleaned in a 0.5% HF solution for 1 min. Around 0.3 nm thick GeO_x IL remains on the surface after the cleaning process.[4] Then the samples were immediately loaded into a home-built ALD chamber through a loadlock. The details for the ALD setup were given in our previous work.[20,21] The Ge surface was passivated by using an NH_3 plasma prior to the ALD growth. An inductively coupled plasma source (remote mode, downstream configuration) was used for generating the plasma. The samples remain stationary in the ALD chamber while the plasma source was separated from the ALD chamber through a computer controlled valve during the precursors pulse time to avoid contamination of the ICP source. The power of the NH_3 plasma was fixed at 200 W with a pressure around 5×10^{-3} mbar and the exposure time was varied from 15 to 30 s. The HfO_2 and TiO_2 dielectric was grown by PE-ALD using either Tetrakis (ethylmethylamido)hafnium(IV) (TEMAH) or tetrakis-dimethyl-amido titanium (TDMAT) and O_2 plasma without breaking a vacuum. A shadow mask was used to pattern sputtered Pt gate electrodes. A Ti(20 nm)/Pt(40 nm) bi-layer structure was used as back electrode to reduce series resistance. Post metal annealing (PMA) was conducted in a forming gas ambient at 300°C for 30 min. Both spectroscopic ellipsometry and X-ray reflectivity (XRR) were employed to measure the thickness of the films. The chemical composition of the film was analyzed by X-ray photoelectron spectroscopy (XPS) using Al Kα x-rays. The capacitance-voltage (C-V) measurement was carried out using an HP 4192 A impedance analyzer. The current was measured with a Keithley 617 electrometer and the applied voltage to the capacitors was calibrated with a HP 3478 A multimeter.

The Ge surface after NH_3 plasma passivation was analyzed by XPS. An ultrathin Al_2O_3 cap layer (~1 nm) was in situ deposited by PE-ALD to avoid contamination and degradation of the formed GeO_xN_y passivation layer. Figure 1 shows the Ge 3d core level spectra. In addition to a doublet attributed to bulk Ge $3d_{3/2}$ and $3d_{5/2}$, the spectra were fitted by three components, GeO, GeO_2 and GeO_xN_y. Except for GeO_xN_y, the chemical shifts of Ge 3d binding energy (BE) for each of these components were fixed according to reported data.[22] The atomic concentration of N in the passivation layer is relatively low and around 8% according to the XPS measurement. Using our current setup for performing the NH_3 plasma treatment, it is difficult to tune the O/N ratio. It is found that the binding energy shift of Ge 3p core level is ~2 eV prior to HfO_2

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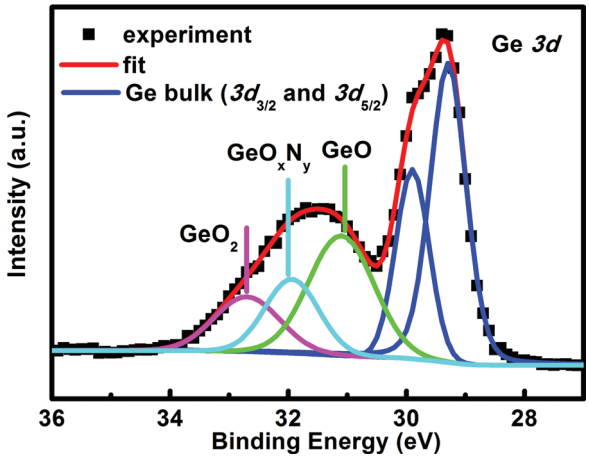

Figure 1. (Color online) (a) XPS Ge 3d spectra for the GeO_xN_y/p-Ge sample capped with an ultrathin Al_2O_3 layer. Two components were extracted: bulk Ge 3d and GeO_xN_y.

deposition and ~1.7 eV after HfO_2 deposition (data not shown), suggesting partial intermixing between the GeO_xN_y layer and the subsequent HfO_2 film. HfO_2 and TiO_2 were grown on the passivated Ge (100) using PE-ALD without air exposure. Hf 4*f* and Ti 2*p* XPS core level spectra are shown in Fig. 2. A doublet with binding energy of 16.4and 18.1 eV was well fitted for Hf 4*f* spectra, which shows oxidation state of Hf^{4+} and no significant contribution from sub-oxide or defects.[23] Similarly, a doublet with binding energy of 464.4and 458.7 eV was extracted for the Ti 2*p* core levels, which is consistent with the TiO_2 component (Ti^{4+}).[23] XPS analysis indicates that the films grown by PE-ALD have very low level of sub-oxide and defects and are suitable for the application of gate stacks. It is attributed to the high reactivity of O radicals created by the O_2 plasma, therefore, resulting in complete oxidation.

Electrical properties of the MOS capacitors with TiO_2/HfO_2 bi-layer gate stacks are comprehensively evaluated. Figure 3 shows the *C-V* and *J-V* characteristics for the capacitor on n-Ge (100) with capacitance equivalent thickness (CET) of ~1.6 nm. A ~1 nm thick GeO_xN_y passivation layer was formed by in situ NH_3 plasma treatment with plasma exposure time of 30 s. The thickness of HfO_2 and TiO_2 was around 1.2 and 3 nm, respectively. Multiple frequencies (from 200 Hz to 1000 KHz) were used to obtain both flat C_{min} at high frequency and response of minority carriers at low frequency (shown in Fig. 3a). Well behaved *C-V* curves suggest effective electrical Ge surface passivation using in situ formed GeO_xN_y layer. The Berglund method was used to relate the Ge surface potential to the gate bias (data now shown).[24] The range of Ge surface potential change is larger than 0.8 eV, which suggests free movement of the Femi-level at the Ge surface through the entire Ge band gap since

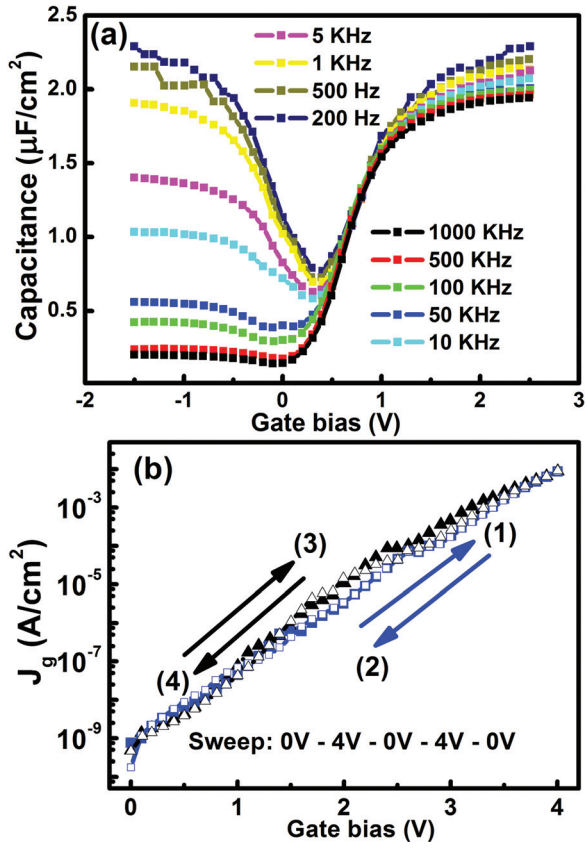

Figure 3. (Color online) (a) *C-V* characteristics (b) *J-V* characteristics of the MOS capacitor with TiO_2(3nm)/HfO_2(1.2 nm)/GeO_xN_y(1 nm) gate stacks on n-Ge (100).

the range is already greater than the Ge band gap (0.66 eV). Therefore, the inversion response is not related to interface-trap-dominated generation-recombination of carriers in inversion, but rather a true inversion behavior. The interface trap density (D_{it}) was also estimated by using the high-low frequency method[25] and it was lower than 7×10^{11} $eV^{-1}cm^{-2}$ at flat-band condition. Very promising device stability against high voltage gate bias was observed for the capacitor with TiO_2/HfO_2 bi-layer stacks. Figure 3b shows high reproducibility of gate leakage current density (J_g) when the gate bias repeatedly sweeps from 0 to 4 V back and forth. The dielectric breakdown voltage was increased substantially from ~3.4 V for the capacitor using a HfO_2 single layer stack to ~4.2 V for the capacitor using TiO_2/HfO_2 bi-layer stacks with similar GeO_xN_y IL and CET of ~1.6 nm.[19] It is related to the fact that one can use a larger

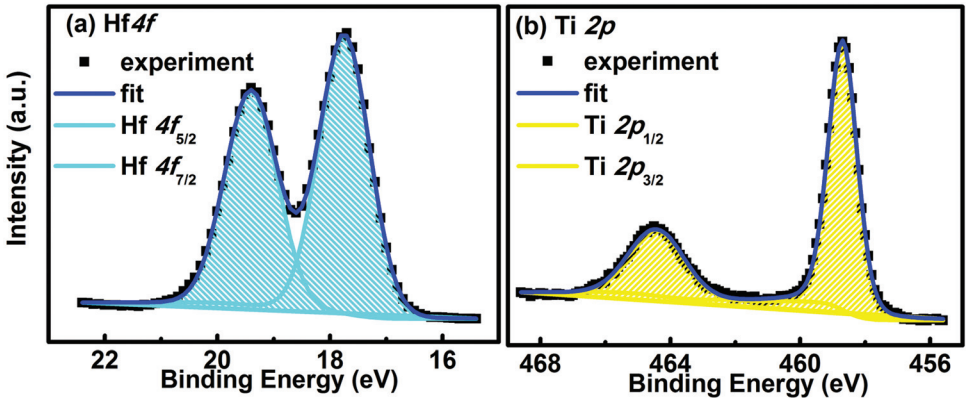

Figure 2. (Color online) (a) XPS Hf 4*f* core level spectra (b) XPS Ti 2*p* core level spectra.

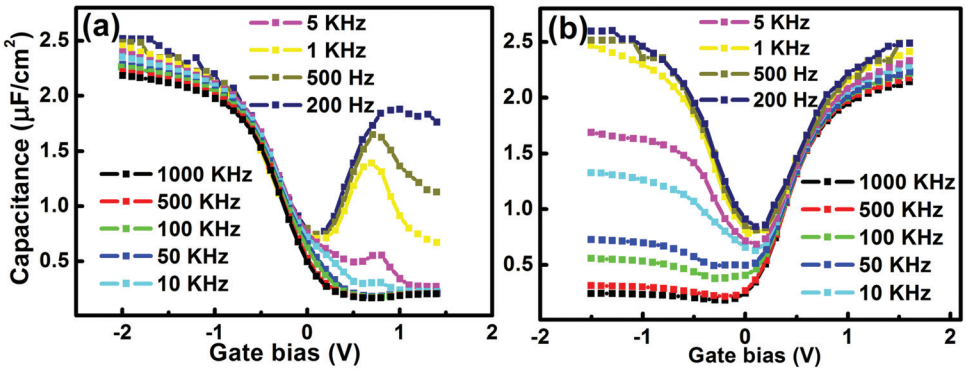

Figure 4. (Color online) *C-V* characteristics of the MOS capacitors with TiO_2(3 nm)/HfO_2(1.2 nm)/GeO_xN_y(0.7 nm) gate stacks on (a) p-Ge (100) and (b) n-Ge (100).

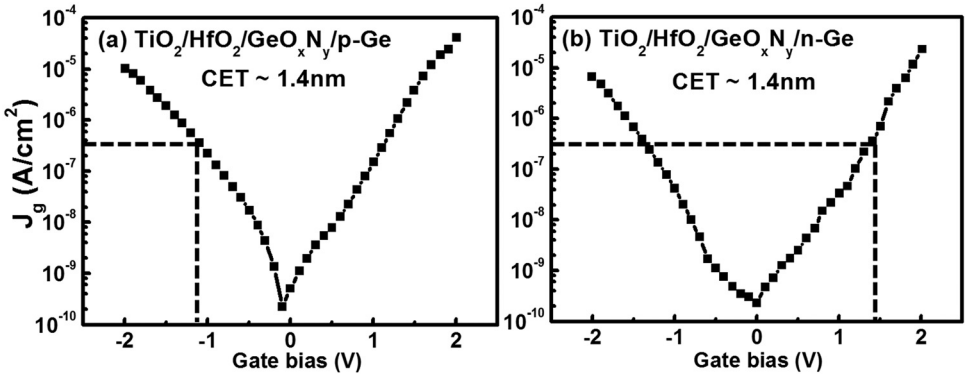

Figure 5. *I-V* characteristics of the MOS capacitors with TiO_2(3 nm)/HfO_2(1.2 nm)/GeO_xN_y(0.7 nm) gate stacks on (a) p-Ge (100) and (b) n-Ge (100).

physical thickness of the TiO_2/HfO_2 bi-layer stacks while maintaining similar EOT since TiO_2 exhibited a higher dielectric constant (~50) than HfO_2 (~24). It is worth mentioning that NH_3 plasma formed GeO_xN_y IL shows a higher dielectric break down field (~15 MV/cm) than O_2 plasma formed GeO_2 IL (~10 MV/cm). *C-V* hysteresis was evaluated to be around 80 mV at flat-band voltage. *C-V* hysteresis is usually attributed to bulk oxide traps related to Ge outdiffusion or interface mixing.[4] The decrease of BE shift of Ge 3*p* core level after HfO_2 deposition (from 2 to 1.7 eV) suggests partial intermixing between the GeO_xN_y layer and the subsequent HfO_2 film, and may causes the hysteresis behavior. However, the outdiffusion of Ge into HfO_2 is limited by using GeO_xN_y IL and in situ PE-ALD HfO_2. According to the XPS measurement, the atomic concentration of Ge in the thin HfO_2 films is less than 3%, which indicates sufficient suppression of Ge outdiffusion.

A minimum CET of 1.4 nm was obtained for capacitors on both p and n-type Ge (100) by reducing the NH_3 exposure time to 15 s, and therefore decreasing the thickness of the GeO_xN_y layer to ~0.7 nm. It is worth mentioning that the "re-growth" of the IL during the PE-ALD process due to the highly reactive O radicals makes it very difficult to further reduce the IL thickness. As shown in Fig. 4, no severe degradation was observed for the capacitor on n-Ge (100) and well shaped *C-V* curves remained. However, apparent *C-V* bumps were demonstrated for the capacitor on p-Ge (100) in an ac frequency range from 5 KHz to 500 Hz. An asymmetric D_{it} distribution and much higher D_{it} at the Ge conduction band side could be the source for such degradation.[26] A similar degradation was observed for TiO_2/HfO_2 bi-layer gate stacks when using a GeO_2 passivation layer.[11] Further investigation is necessary to determine the mechanism of the degradation and for optimizing the capacitors on p-Ge (100). Nevertheless, low J_g ($<4 \times 10^{-7}$ A/cm^2) was obtained for both capacitors at $V_{FB} \pm 1$ V with a CET of 1.4 nm as shown in Fig. 5. It opens perspective for continued EOT scaling while maintaining a low J_g.

In summary, we found that TiO_2 and HfO_2 thin films grown by PE-ALD exhibit no significant sub-oxide components or defects. Excellent stability was demonstrated for the capacitors with TiO_2/HfO_2 bi-layer gate stacks against high voltage gate bias. The capacitor can sustain repeated gate bias sweeps from 0 to 4 V at CET around 1.6 nm. With decreasing thickness of the GeO_xN_y IL, low J_g ($<4 \times 10^{-7}$ A/cm^2) was obtained at $V_{FB} \pm 1$ V for the capacitors on both p and n-type Ge(100) with a minimum CET of 1.4 nm. However, degradation in the inversion region was observed for the capacitor on p-Ge (100).

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